HEWLETT PACKARD

Analyzing the Motorola 6809/6809E

(HP 1650A/51A and HP 16510A Logic Analyzers) Model 10308B

Operating Note/August 1987

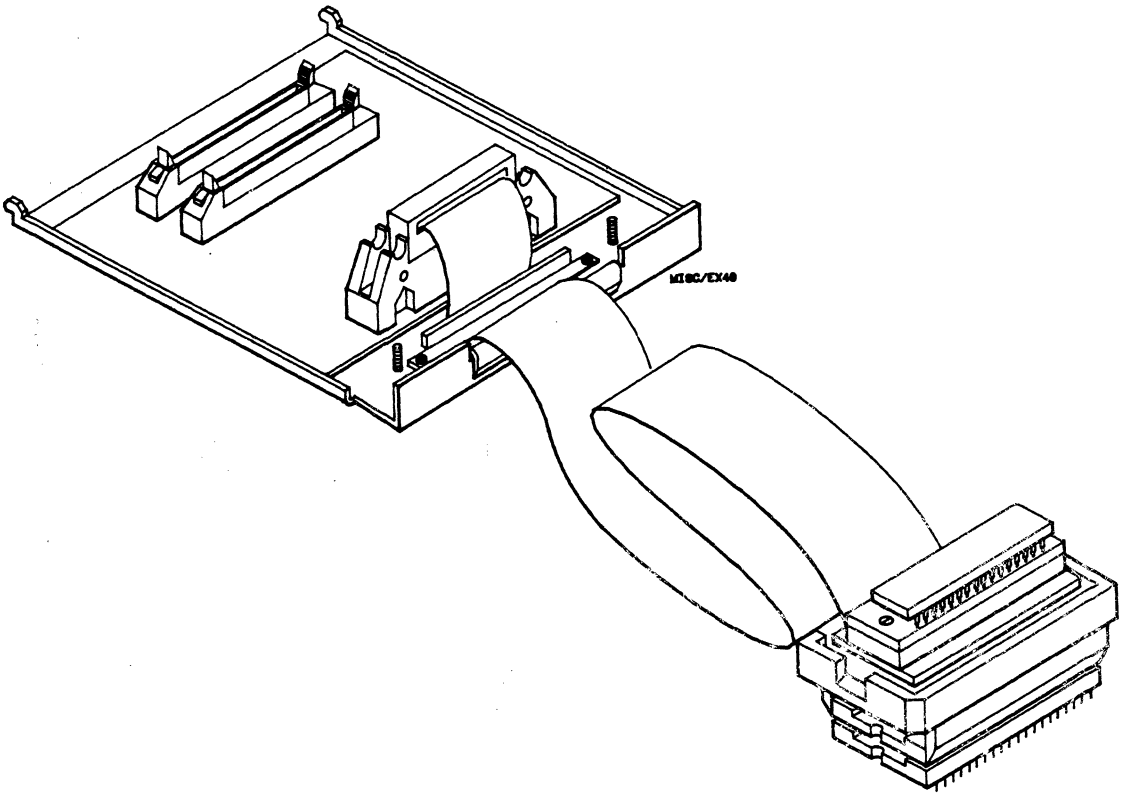

Figure 1. HP 10308B Preprocessor

Introduction

This operating note includes information on using the 6809/6809E Inverse Assembler with or without the HP 10269C and HP 10308B Preprocessor Interface Module.

Operating Note Part No. 10308-90910
Microfiche Part No. 10308-90810

Table of Contents

Table of Contents (Continued)

Installation Overview

1. Set the CPU/MMU switches on the HP 10308B to the CPU position (see page 6).
2. Install the 6809/6809E Preprocessor (HP 10308B) in the HP 10269C General Purpose Probe Interface (see page 6).
3. Connect the 6809/6809E preprocessor cable to the target system (see page 8).
4. Plug the logic analyzer probes into the probe interface as follows:

HP 1650A/51A and 16510A Pod	(into)	HP 10269C Connector
1		1
2		2

5. Load the logic analyzer configuration and inverse assembler by loading file C6809_I from the inverse assembler disc (see page 11).

Analyzing the 6809/6809E with the HP 10308B

The HP 10308B Preprocessor and Inverse Assembler consists of the following:

* the preprocessor hardware, which includes the interface circuit card and cable assembly;
* the inverse assembly software on a 3-1/2-inch disc; and
* this operating note.

The HP 10308B Preprocessor Interface Module, when installed in the HP 10269C General Purpose Probe Interface, provides a complete interface between any 6809/6809E target system and the HP 1650A, HP 1651A, or HP 16510A Logic Analyzer. The interface module connects the signals from the 6809/6809E target microprocessor to the logic analyzer inputs and generates all status and clock signals required by the software for inverse assembly of the 6809/6809E instruction set.

The 6809/6809E configuration software on the flexible disc sets up the Format Specification menu of the logic analyzer for compatibility with the 6809/6809E microprocessor. It also loads the inverse assembler for obtaining displays of 6809/6809E data in 6809 assembly language mnemonics. The interface module specifications are given in Appendix A.

Equipment Required

The minimum hardware required for state analysis of a 6809/6809E target system consists of the following:

* An HP 1650A, HP 1651A, or HP 16510A Logic Analyzer;
* The HP 10269C General Purpose Probe Interface, which connects the preprocessor to the logic analyzer; and
* The 6809/6809E Preprocessor and Inverse Assembler (HP 10308B).

Connecting the HP 10308B to the HP 10269C

The HP 10269C routes the signals from the HP 10308B Preprocessor and provides the correct mechanical connections for the logic analyzer probes. To connect the HP 10308B to the HP 10269C:

Note

There are six switches on the HP 10308B which select either CPU (logical) or MMU (physical) address bits to be sent to the logic analyzer for analysis. For initial installation, these switches must be in the "CPU" position. The CPU and MMU positions are etched on the printed circuit board. Refer to "Probing Additional Analysis Channels" on page 20 of this operating note before setting any of these switches to the MMU position.

1. Install the HP 10308B Interface Module Card on the underside of the HP 10269C General Purpose Probe Interface Pod (see figure 3).

2. Insert the free end of the interface card in the slots of the pod.

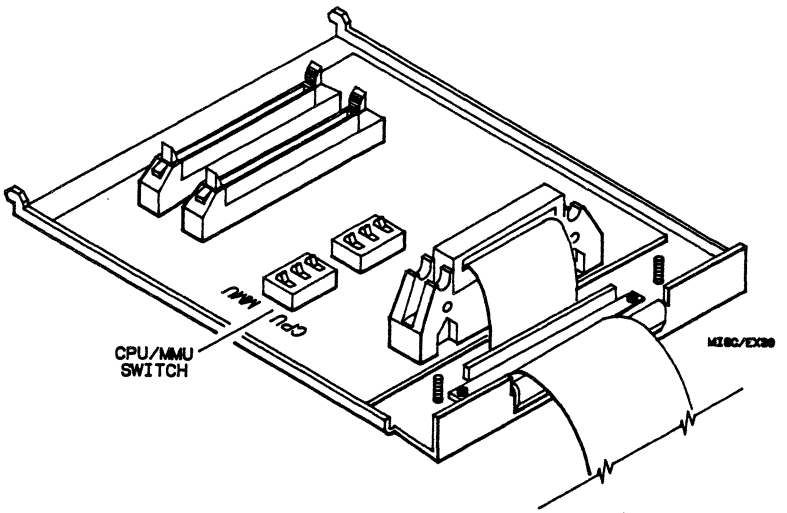

Figure 2. Location of the CPU/MMU Switches

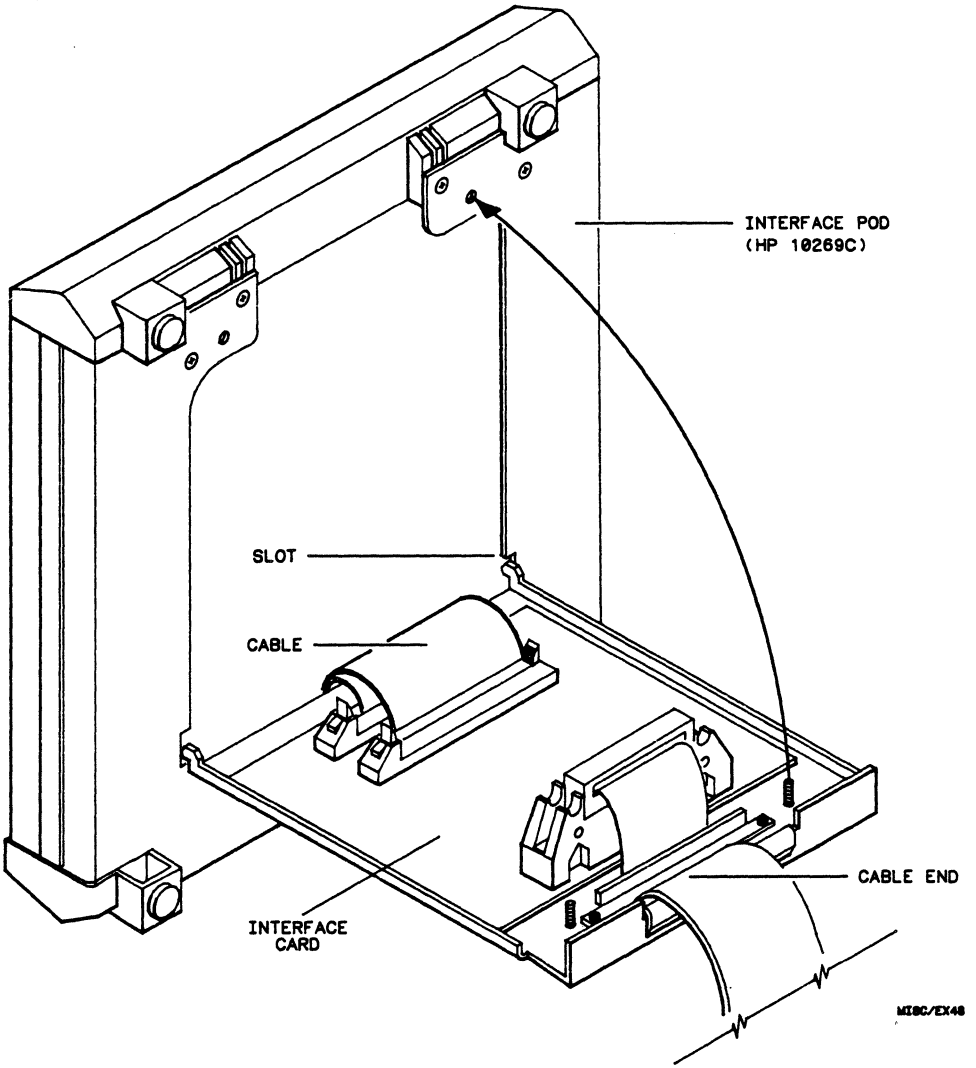

Figure 3. Mounting the HP 10308B on the HP 10269C

3. Connect the two pod internal cables to the interface circuit card.

4. Gently fold the interface card into the pod and fasten the cable end of the interface card to the pod using two screws.

CAUTION

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the interface module or microprocessor is being connected or disconnected.

Connecting to the Target System

1. Remove the 6809/6809E microprocessor from its socket on the target system and store it in a protected environment.

2. Plug the interface cable into the microprocessor socket on the target system.

CAUTION

Care must be taken to align pin 1 of the cable assembly with pin 1 of the microprocessor socket on the target system to prevent mis-alignment or damage. Pin 1 of the cable socket is identified on the socket board and shown in figure 4.

3. The microprocessor socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the microprocessor, open the socket by rotating the small screw counterclockwise on the pin 1 end of the socket.

4. Plug the 6809/6809E microprocessor into the socket of the interface cable.

5. Secure the microprocessor in the socket by rotating the screw on the socket clockwise.

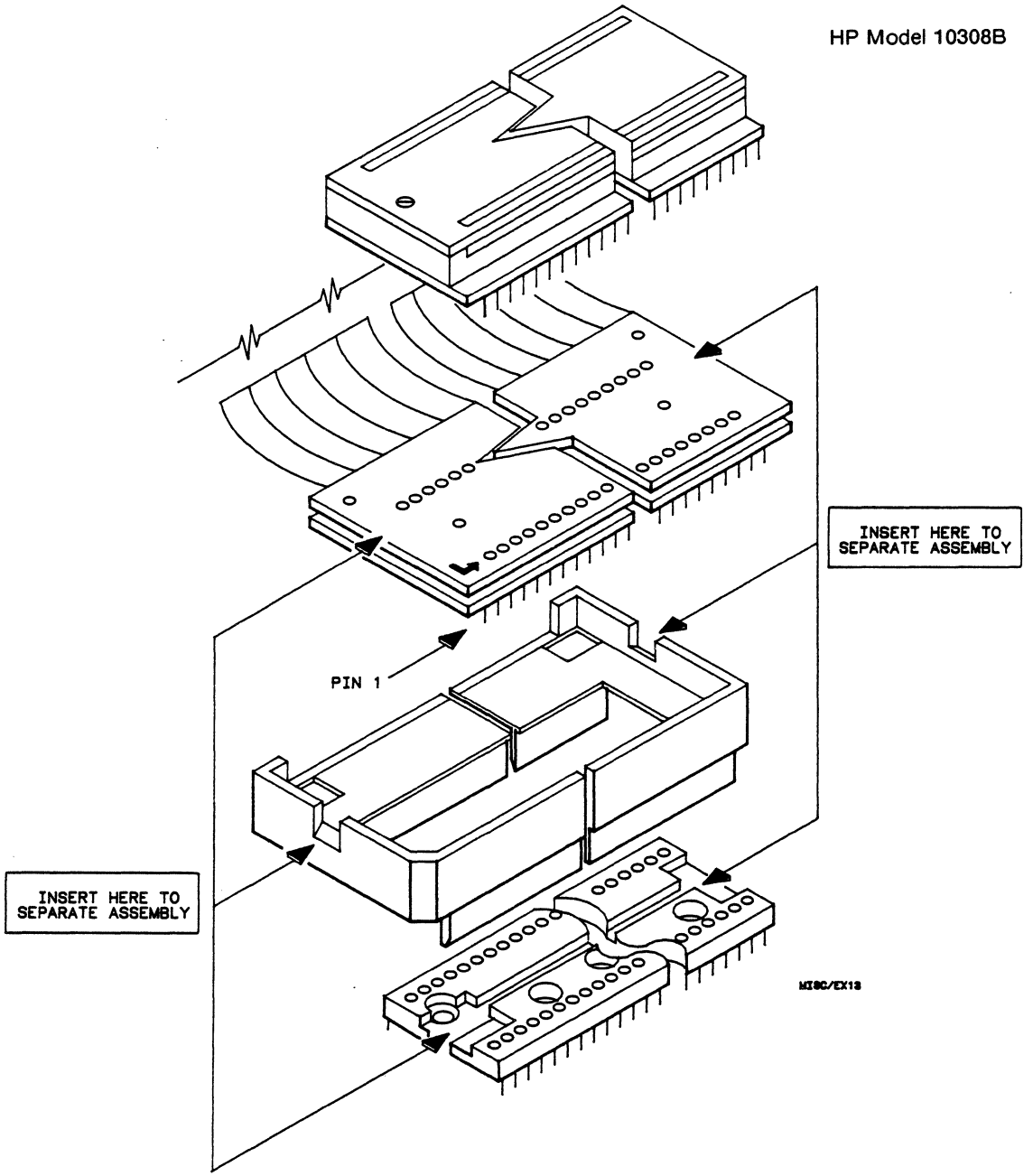

Figure 4. ZIF Socket Assembly (Exploded View)

Note

The ZIF socket assembly pins, shown in figure 4, are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done for two reasons:

1. To protect the user interface circuitry in the preprocessor from electrostatic discharge (ESD); and

2. To protect the delicate gold plated pins of the assembly from damage due to impact.

When you're not using the preprocessor, protect the socket assembly pins from damage or ESD by covering them with the foam or plastic pin protector.

For a lower profile assembly, use the probe without the ZIF socket.

1. Separate the ZIF socket assembly by inserting a flat blade screw driver under the PC board located directly below the ZIF socket and carefully prying up the ZIF socket (see figure 4). Avoid bending the pins of the ZIF socket or interface cable assembly.

CAUTION

Removing the ZIF socket assembly is not recommended because it increases the danger of damaging the 6809 microprocessor or microprocessor socket on the interface cable.

2. Plug the interface cable into the target system.

3. Install the microprocessor in the socket of the interface cable.

Note

The plastic pin guard can be removed if it interferes with components of the target system or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damaging the pins on the interface assembly.

Connecting to the HP 10269C

Connect the HP 1650A, HP 1651A, or HP 16510A Logic Analyzer pods to the HP 10269C General Purpose Probe Interface as follows:

HP 1650A/51A and 16510A Pod	(into)	HP 10269C Connector
1		1
2		2

Setting Up the Analyzer from the Disc

The logic analyzer can be configured for 6809 or 6809E analysis by loading the configuration file C6809_I from the flexible disc. Loading this file will also load the inverse assembler file. To load the configuration and inverse assembler:

1. Install the flexible disc labeled "6809/09E Inverse Assembler for use with: HP 1650A, HP 1651A, and HP 16510A" in the front disc drive of the logic analyzer.

2. Select the I/O Disc Operations menu on the HP 1650A or HP 1651A, or the Front Disc menu of the System menu on the HP 16510A.

3. Configure the menu to "Load" the analyzer from the file C6809_I.

4. Then execute the load operation to load the file into the HP 1650A, HP 1651A, or HP 16510A.

Slow Clock

If you have the interface module hooked up and running and observe a slow clock or no activity on any pods of the interface board, check the +5 V supply coming from the analyzer. To do this:

Disconnect one of the logic analyzer cables from the HP 10269C and measure across pins 1 and 2 (see figure 5).

* If +5 V isn't observed across these pins, check the internal preprocessor fuse on the HP 1650A, HP 1651A, or HP 16510A Logic Analyzer. For information on checking this fuse, refer to the HP 1650A/51A or HP 16510A service manuals.

* If +5 V is observed across these pins and you feel confident that the +5 V is getting to the interface module, then the interface module is most likely the problem. If this is the case, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

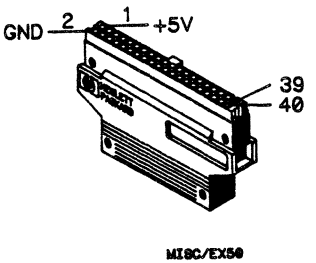

Figure 5. Pinout for the Logic Analyzer Cable

Format Specification

When you use the 6809/6809E Interface Module, the format specification will automatically be set up by the flexible disc software as in figure 6.

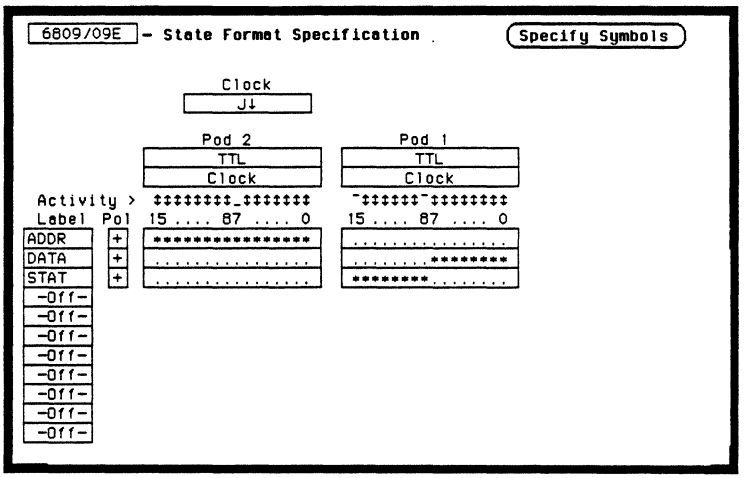

Figure 6. Format Specification for 6809/6809E

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The ADDR, DATA, and STAT labels are used by the inverse assembler to generate assembly language mnemonics for display in the trace list. Pertinent control and clock threshold levels are also part of the format specification.

The J clock is normally used to clock the logic analyzer. This signal is active for all 6809 cycles that are useful for state analysis. Unused or fetch ahead cycles made by the microprocessor, as well as sync acknowledge and halt/bus grant cycles, are not sent to the logic analyzer with the J clock. Use the K clock to look at bus cycles that are not included in the J clock. This clock is the buffered 6809 Q line.

Symbols Menu

The Symbols menu of the format specification is set up with names to identify values found on the status label (see figure 7).

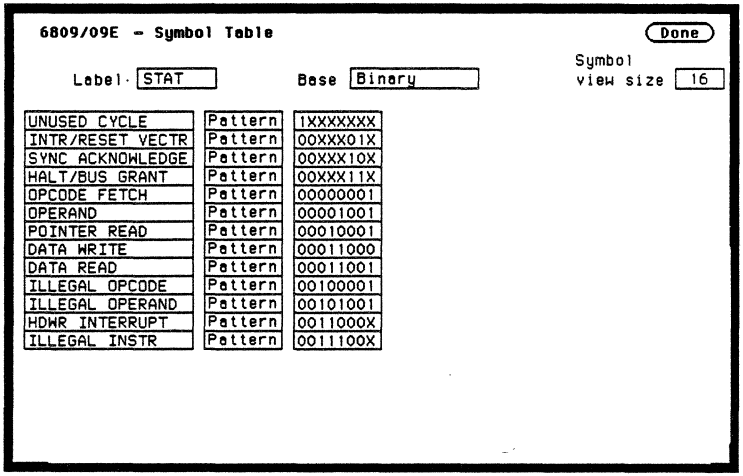

Figure 7. Symbols Menu for the 6809/6809E

Listing Menu

Captured data is displayed as shown in figure 8. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

6809/09E - State Listing

Markers Off

Label >	ADDR	6809/6809E Mnemonic		STAT
Base >	Hex		hex	Symbol
+0000	F800	LDS	#0400	OPCODE FETCH
+0001	F801	CE	program read	OPERAND
+0002	F802	04	program read	OPERAND
+0003	F803	00	program read	OPERAND
+0004	F804	LDD	#1000	OPCODE FETCH
+0005	F805	10	program read	OPERAND
+0006	F806	00	program read	OPERAND
+0007	F807	LDX	#1000	OPCODE FETCH
+0008	F808	10	program read	OPERAND
+0009	F809	00	program read	OPERAND
+0010	F80A	LDY	#1000	OPCODE FETCH
+0011	F80B	8E	program read	OPERAND
+0012	F80C	10	program read	OPERAND
+0013	F80D	00	program read	OPERAND
+0014	F80E	LDU	#1000	OPCODE FETCH
+0015	F80F	10	program read	OPERAND

Figure 8. Listing Menu for the 6809/6809E

The 6809/6809E Inverse Assembler

The 6809/6809E Inverse Assembler has been constructed so mnemonic output will resemble actual assembly source code. Numerical values such as addresses and immediate values are normally displayed in hexadecimal format. The one exception is the immediate value for the ANDCC and ORCC instructions that are displayed in binary form, making it easier to determine which bits are being modified in the condition code register.

Interpreting Data

The pair of asterisks (**) displayed in the operand field of an instruction indicate that a byte of an expected operand was not stored in analyzer memory. Four asterisks (****) indicate that two bytes of an expected operand were not stored.

Examples:

LDA	#**	(missing byte operand)
JMP	23**	(missing low byte of address)
JMP	****	(missing both bytes of address)

In general, asterisks indicate that expected operand fetches are not stored in analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace and format specifications.

Error Messages

The following messages will appear with program errors.

Illegal Instruction - unidentified opcode encountered on the first byte or on the second byte if the first byte is 10H or 11H

Illegal Postbyte - the register mask for a transfer or exchange instruction, or an illegal indexed addressing mode

Undefined Bus Cycle - the combination of bus available (BA), bus status (BS), and read/write (R/W) is not recognized for the 6809/6809E

Note

Do not modify the ADDRESS, DATA, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results.

Analyzing the 6809/6809E Directly with the Logic Analyzer Probes

In order to use the inverse assembler for probes, the general purpose probes must be connected to the 6809/6809E microprocessor as shown in table 1. After the specified hookups have been completed, data sampling may begin. Load file C6809_P for analyzing a 6809 microprocessor and file C6809E_P for analyzing a 6809E microprocessor. When the disc is read, the format specification for the 6809/6809E is automatically set up. This format specification corresponds with the hookup specification.

The 6809 and 6809E do not provide enough status information to identify the first byte of an instruction fetch in a series of program reads. The HP 10308B Interface Module generates additional status information to allow the inverse assembler to disassemble captured data automatically.

When a 6809 or 6809E are probed without the HP 10308B, the logic analyzer cannot identify the first byte of an instruction fetch. When you are using the general purpose probes, you must point to the first byte of an instruction fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

To do this:

1. Select a line on the display that you know is the first state of an instruction fetch.

2. Roll this line to the top of the listing.

3. Select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

Rolling the screen up will inverse assemble the lines on the bottom of the screen as they appear on screen. If you jump to another area of the screen by entering a new line number, you must re-synchronize the inverse assembler by repeating steps 1 through 3.

Note

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in analyzer memory, but the activity between those blocks will not be inverse assembled.

Table 1. Connecting Directly to the 6809/6809E with Logic Analyzer Probes

HP 1650A/51A and 16510A		6809/6809E		
Pod	Probe	Pin	Pin Mnemonic	Label
1	J CLK	34	CLK E	CLOCK
2	0	8	A0	ADDRESS
2	1	9	A1	ADDRESS
2	2	10	A2	ADDRESS
2	3	11	A3	ADDRESS
2	4	12	A4	ADDRESS
2	5	13	A5	ADDRESS
2	6	14	A6	ADDRESS
2	7	15	A7	ADDRESS
2	8	16	A8	ADDRESS
2	9	17	A9	ADDRESS
2	10	18	A10	ADDRESS
2	11	19	A11	ADDRESS
2	12	20	A12	ADDRESS
2	13	21	A13	ADDRESS
2	14	22	A14	ADDRESS
2	15	23	A15	ADDRESS
1	0	31	D0	DATA
1	1	30	D1	DATA
1	2	29	D2	DATA
1	3	28	D3	DATA
1	4	27	D4	DATA
1	5	26	D5	DATA
1	6	25	D6	DATA
1	7	24	D7	DATA
1	8	32	R/W	STATUS
1	9	5	BS	STATUS
1	10	6	BA	STATUS

Probing Additional Address Channels (HP 1650A and HP16510A)

6809/6809E systems often use a memory management unit to expand the addressing capabilities of the microprocessor. The interface module has been designed to allow you to monitor these address lines with the logic analyzer while continuing to monitor the 6809/6809E address lines. Since the HP 1650A or HP 16510A provide additional unused pod lines, probing additional address lines is possible.

Address Lines

Additional address lines are defined as lines that are located above the 16 microprocessor address lines. Together, with the 16 microprocessor address lines, an address field greater than 16 bits is formed. The additional address lines can be generated by a variety of methods and are defined entirely by the target system.

Included on the interface is circuitry that will sample up to eight additional address lines at the end of the bus cycle (the falling edge of the E clock), along with other information from the 6809/6809E microprocessor. In addition, an area at the top of the interface board has been defined which allows these lines to connect from the target system to the logic analyzer in a convenient manner.

To monitor the additional address lines, you must first be connected to the interface module. A standard ribbon cable with a maximum of 50 conductors is recommended for this purpose. A connector of the same type used for the 6809/6809E probe cable (connector J1) should be installed at the very top of the interface board at the location labeled "J2." Just below this area is a group of pins labeled "MMU ADDRESS." In the resulting address field received by the analyzer, the numbers 10 through 23 represent the bit position for each pin. Bit 10 is the least significant position in this group. Using wire-wrapping techniques, connect the appropriate pins of the USER DEFINABLE CABLE to the MMU ADDRESS inputs. Inputs 16 and higher should be used for the additional address lines, with the size of the label ADDRESS in the format specification increased appropriately. Additional explanation is given in the following paragraphs. Verify that all six switches on the interface board are in the CPU position. Note the outline, etched on the printed circuit board, which shows the switch position.

Memory Management Unit Lines

A Memory Management Unit (MMU) typically receives some of the higher microprocessor address lines, maps these lines, and generates a larger group of lines. This group, together with the lower address lines from the microprocessor, form an address group that has more than 16 bits. This new address is often called the physical address, whereas the 16-bit address from the microprocessor is called the logical address. If you want to enter the physical address in the logic analyzer, instead of the logical address, you need to overlay some of the higher address lines from the microprocessor with lines from the MMU. The HP 10308B Interface Module allows address lines A10 through A15 to be replaced with lines from the MMU. This selection is made on an individual address line basis with switches on the interface board.

To monitor a physical address with the logic analyzer, connect the desired lines to the interface via the USER DEFINABLE CABLE described in the previous paragraphs. Using wire-wrapping techniques, connect the physical address lines produced by the MMU to the appropriate MMU ADDRESS pins. Numbers 10 through 23 refer to the bit position in the resulting 24 bit physical address, with bit 10 being the least significant bit in the group. Signals input to positions 10 through 15 will replace the corresponding address lines from the microprocessor when the switches for those bits are placed in the MMU position. Note the outline showing the switch position that is etched on the printed circuit board. The switch closest to the top of the interface board is for address line A10, and the switch nearest the bottom of the board is for address line A15. All other switches are not labeled, but are in numeric order from A10 through A15.

To set up the logic analyzer:

1. Plug pod 3 from the logic analyzer into "POD 3" on the top of the HP 10269C.

2. In the Configuration menu of the logic analyzer, assign pod 3 to Analyzer 1 (machine 1).

3. In the Format menu, add the additional address channels from the MMU to the ADDR label. The eight additional address channels come in on the least significant eight bits of pod 3. The format specification for a 6809 system with a 24-bit physical address is shown in figure 9.

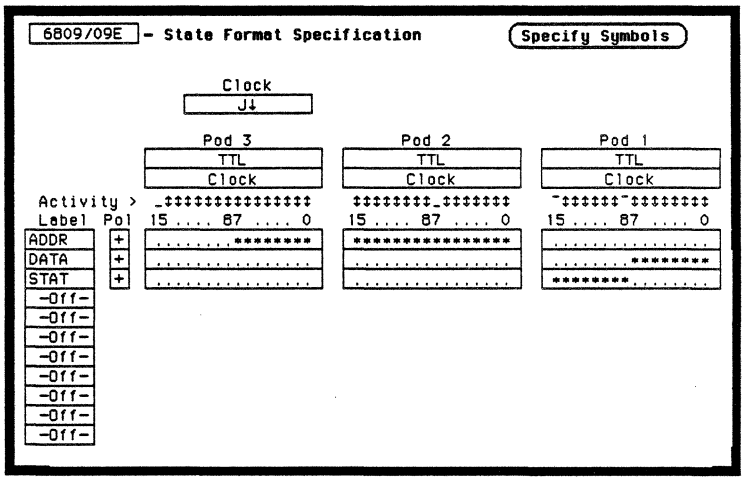

Figure 9. Format Menu for the 6809/6809E with Additional Address Lines

A General Information

Interface Module Specifications

Microprocessor Compatibility: Motorola 6809/6809E and all microprocessors made by other manufacturers that comply with the Motorola 6809/6809E specifications.

Microprocessor Package: 40-pin DIP

Accessories Required: HP 10308B and HP 10269C

Maximum Clock Speed: 2 MHz Clock Input

Signal Line Loading: 1 LS TTL load + 35 pF on the following lines:

A15-A0, D7-D0, R/LW, BS, BA, QCLK, ECLK

Microprocessor Operations Displayed:
Memory Read/Write
DMA Read/Write
Opcode Fetch/Operand
Vector Fetch
Halt
Interrupt

Additional Capabilities: The preprocessor can be adapted to 6809/09E systems that use a Memory Management Unit (MMU). This adaptation allows the capture of addresses on a Physical Address Bus up to 24 bits wide.

Power Requirements: 1.0 A at +5 Vdc, supplied by the logic analyzer

Logic Analyzer Required: HP 1650A, HP 1651A, or HP 16510A

Number of Probes Used: Two 16-channel probes

Environmental

Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F)
	Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F)
Altitude:	Operating, 4600 m (15,000 ft)
	Nonoperating, 15,300 m (50,000 ft)
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Interface Description

The primary function of the interface module is to connect the 6809/6809E target microprocessor to the logic analyzer through the general purpose probe interface and to perform any required functions unique to the HP 10308B Interface Module.

Signals from the target system are sampled at the end of each cycle, at the Bus Latch. The control logic receives the E and Q clock signals and the BA, BS, and R/LW status lines from the microprocessor as inputs, then produces several signals. First, two signals are generated to clock the logic analyzer. Normally the J clock is used as the signal and is active for each microprocessor cycle that is useful for analysis. The status generator determines these cycles. The K clock is active for every cycle of the E and Q clocks. The negative edge of both the J and K clocks is used to clock the logic analyzer. For a given bus cycle, this will occur at the negative edge of Q on the following bus cycle.

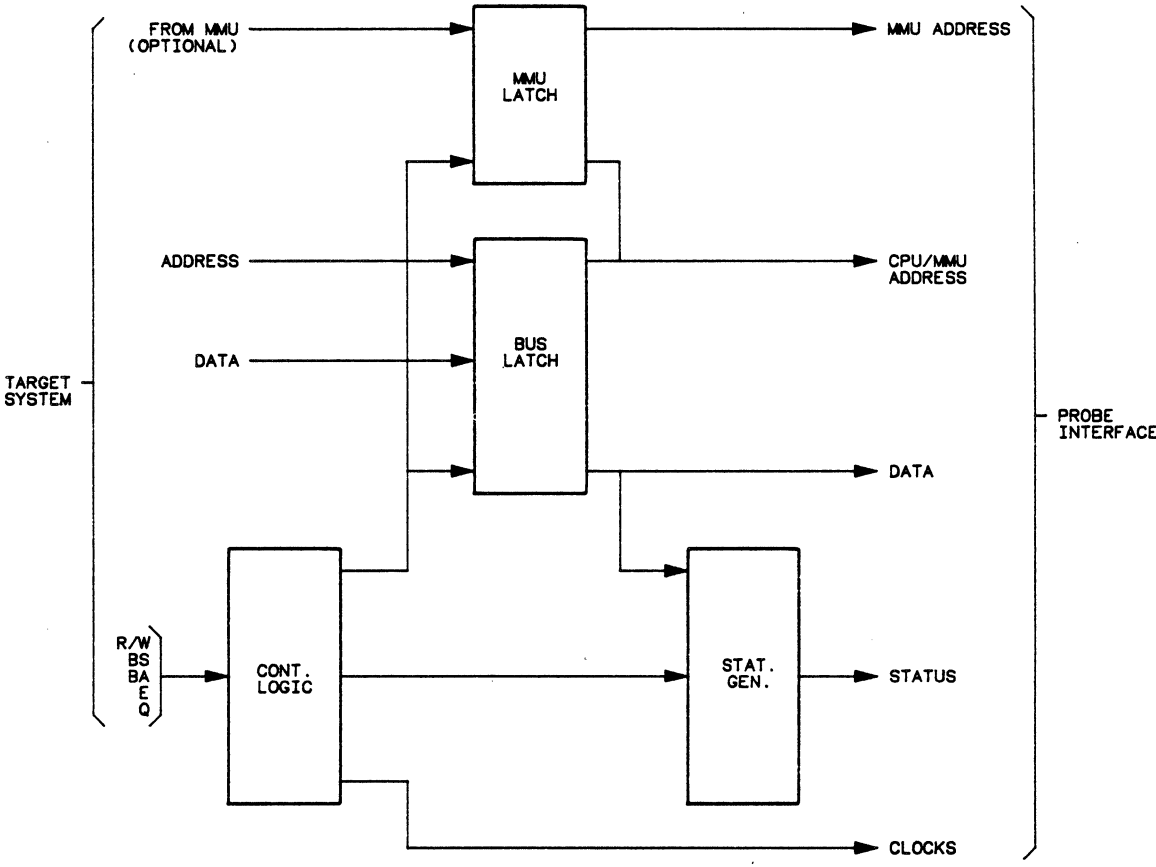

Figure A-1. 6809/6809E Interface Block Diagram

Status Generation

Another function of the interface module is to generate status information about microprocessor activity which is unavailable from the microprocessor itself. This additional status is generated by a state machine on the interface that tracks all bus cycles and decodes instructions. The type of status generated identifies opcodes, other code bytes, data transfers, unused bus cycles, illegal instructions, and other types of cycles. How to use status generated by the interface is described later in this operating note.

Status Field Encoding

There are eight bits in the complete status field that may be divided into two groups. The lower three bits are status lines available from the 6809/6809E. The upper five bits are generated by circuitry on the interface module. The eight bits are defined as follows:

Bit 7 = 0 for cycles that are needed for analyzing 6809/6809E instruction execution;

Bit 7 = 1 for non-valid, fetch ahead, sync acknowledge, halt, or non-microprocessor cycles;

Bit 6 is always low

Bits 5 through 3 are generated by the interface module and are encoded together for the following actions:

000 = first byte of an instruction (opcode)

001 = second byte or following byte of an instruction

010 = the pointer fetch indirect addressing mode

011 = data read or write as the result of instruction execution

100 = illegal first byte of an instruction

101 = illegal second or following instruction byte

110 = instruction interrupted by hardware interrupt (this status is only given on the second cycle of an instruction)

111 = no status generated due to the fetch of an illegal instruction (status generation will resume with a microprocessor write or reset/interrupt vector read cycle)

Bit 2 is the 6809/6809E BA line

Bit 1 is the 6809/6809E BS line

Bits 1 and 2 are encoded for the following states:

00 = normal (microprocessor executing instructions)

01 = vector fetch, reset, or interrupt

10 = sync acknowledge

11 = halt or bus grant

Bit 0 is the 6809/6809E R/W line

0 = write cycle

1 = read cycle

Using Status Generated by the Interface

When status from the microprocessor indicates a normal running operation (i.e., BA=0, BS=0), the only other status indicated by the microprocessor is whether the transfer is to or from memory. This status does not identify whether the transfer is an opcode fetch, a subsequent code byte, or a data transfer due to instruction execution. The missing information is generated, however, by circuitry on the interface module, and given to the logic analyzer, along with the address and data for each bus cycle. This additional status information is particularly useful in analyzing program activity because the information is generated in real time, allowing the logic analyzer to trigger or store qualify on various types of bus cycles that are not identified by the microprocessor.

Status Codes

There are five different status codes used by the interface module to identify most bus cycles of the 6809/6809E microprocessor. The five types of cycles are defined as:

Type	Description	Bits 7 5 4 3
Opcode	the first byte of any instruction (the opcode mnemonic will be displayed in place of the word opcode).	0 0 0 0
Program	the second or following byte of any instruction.	0 0 0 1
Pointer	the two byte pointer fetched during an indirect addressing mode instruction.	0 0 1 0
Data	the memory read or write due to program execution.	0 0 1 1
Unused	a cycle which has no value for the logic analyzer.	1 X X X

With this additional status information, defining trace specifications is easier and more specific. For example, the analyzer can be triggered on an opcode fetch from an address outside the known legal range for instructions. Once a "center on" or "end on" trace has been specified, the cause of the microprocessor's illegal program transfer can be determined. A much larger picture of program activity may be captured with a single trace by storing only opcodes.

When a bus cycle that has no value for state analysis is encountered during normal program execution, the status label "unused" is issued to the logic analyzer. This information is normally not stored in analyzer memory. These unused cycles are withheld from the logic analyzer by clocking the analyzer with the J clock. The falling edge of the K clock must be used when it is necessary to see the "unused" cycles. The following paragraphs identify some types of "unused" cycles that may occur.

Since the microprocessor performs either a memory read or write for each cycle of the E clock, some of the memory reads are redundant. When the microprocessor fetches an instruction, it may fetch one or more bytes of the next instruction. These bytes are fetched before the instruction has been completely decoded, therefore, some of the bytes are unnecessary and discarded. These discarded bytes may be fetched again if the next instruction is executed. Discarded bytes are identified by the interface module as "unused" cycles. "Unused" cycles may prevent a read to a legitimate address in analyzer memory.

Other unused bus cycles occur when the microprocessor is performing an internal operation which takes one or more clock cycles. During this time the microprocessor will read from memory location OFFFFH and the interface module will identify these cycles as "unused". Because this identification is not based solely on the address OFFFFH, a valid data read from address OFFFFH will not be labeled "unused."

If an instruction begins with either 10H or 11H, there must be a second byte to define which instruction is to be executed. If the second byte is also 10H or 11H, the microprocessor ignores the data value and continues reading from memory until a value which is not 10H or 11H is found for the second instruction byte. If a string of 10H or 11H data values occurs, such as in a dynamic memory refresh subroutine, the second and following values of 10H or 11H are labeled "unused" by the status generator on the interface module.

Illegal and Interrupted Instructions

The status generator on the interface module will detect and identify illegal instructions. Instructions that can be determined as illegal on the first byte will be labeled illegal opcodes. Instructions that begin with 10H or 11H, but have an illegal second byte, will have the first byte labeled as an opcode, but the second byte will be labeled as an illegal program byte. If the postbyte that specifies the addressing mode in an indexed addressing mode instruction is illegal, then the postbyte will be given a status value of illegal program. Illegal postbytes in transfer and exchange instructions are not detected.

If the microprocessor receives and services an external interrupt, the current program counter will be saved, and an interrupt vector will be fetched. Before the program counter is saved, however, the microprocessor will begin to fetch the next instruction of the interrupted program, but then will abort its execution. The first cycle of the aborted instruction will be labeled as an opcode by the status generator, but the second cycle will be labeled "interrupt." This helps identify the instruction as the first to be executed after the interrupt service routine.

Note

Do not modify the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that modifying the trace specification to store only selected bus cycles may result in incorrect or incomplete inverse assembly.

Target System Load

The interface module was designed to place a minimum electrical load on the target system. All lines that are monitored by the interface will load the target system with one ALS TTL load and approximately 35 pF of capacitance.

The lines include the address and data bus; BA, BS, R/W status lines; and E and Q clock lines. The two pins (38 and 39) that connect to the 6809 on-chip oscillator have only a 1 or 2 pF capacitance load that should not interfere with the oscillator. All other signal carrying lines are connected to the probe cable, but not to any circuitry on the interface module. These have a load of approximately 25 pF.

Clamping Diodes

To protect the interface from being damaged by electrostatic discharge, clamping diodes have been provided on the HP 10308B interface board. These diodes clamp the input voltages from the probe cable to the +5 volt power supply and to ground at the microprocessor. Because of these diodes, the 6809/6809E signal is clamped to ground if the logic analyzer and interface are not powered up, preventing the target system from operating.

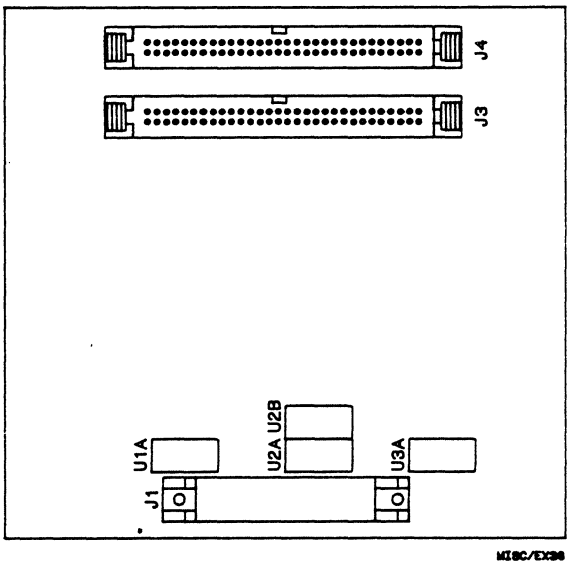

Figure A-2. Location of Clamping Diodes

If the logic analyzer cannot be powered up when the target system is operating, the diode arrays (U1A, U2A, U2B, and U3A) may be removed from their sockets to allow microprocessor operation. However, removal of the diode arrays will increase the susceptibility of the interface module to damage from electrostatic discharge.

Table A-1 lists the microprocessor signals and cable lines on which those signals are carried to the logic analyzer.

Table A-1. 6809/6809E Signal List

CPU Signal	CPU Pin	Label	HP 1650A/51A and 16510A	
			Pod	Bit
(Note 1)		(Clock)	1	J CLK
Q	35	(Clock)	2	K CLK
A0	8	ADDRESS	2	0
A1	9	ADDRESS	2	1
A2	10	ADDRESS	2	2
A3	11	ADDRESS	2	3
A4	12	ADDRESS	2	4
A5	13	ADDRESS	2	5
A6	14	ADDRESS	2	6
A7	15	ADDRESS	2	7
A8	16	ADDRESS	2	8
A9	17	ADDRESS	2	9
A10	18	ADDRESS	2	10
A11	19	ADDRESS	2	11
A12	20	ADDRESS	2	12
A13	21	ADDRESS	2	13
A14	22	ADDRESS	2	14
A15	23	ADDRESS	2	15

Note 1: This clock line has timing similar to the 6809 Q line, but is active only for cycles needed for state analysis.

Table A-1. 6809/6809E Signal List (Continued)

CPU Signal	CPU Pin	Label	HP 1650A/51A and 16510A	
			Pod	Bit
A16	(Note 2)	ADDRESS	3	0
A17	(Note 2)	ADDRESS	3	1
A18	(Note 2)	ADDRESS	3	2
A19	(Note 2)	ADDRESS	3	3
A20	(Note 2)	ADDRESS	3	4
A21	(Note 2)	ADDRESS	3	5
A22	(Note 2)	ADDRESS	3	6
A23	(Note 2)	ADDRESS	3	7
D0	31	DATA	1	0
D1	30	DATA	1	1
D2	29	DATA	1	2
D3	28	DATA	1	3
D4	27	DATA	1	4
D5	26	DATA	1	5
D6	25	DATA	1	6
D7	24	DATA	1	7
R/W	32	STATUS	1	8
BS	5	STATUS	1	9
BA	6	STATUS	1	10
(Note 3)	27	STATUS	1	11
(Note 3)		STATUS	1	12
(Note 3)		STATUS	1	13
(Note 3)		STATUS	1	14
(Note 3)		STATUS	1	15

Note 2: These lines are only used when you are probing additional address lines from a Memory Management Unit.

Note 3: These five status lines are generated by circuitry in the interface module.

Interface Requirements

The HP 10308B Interface Module operates with a 6809/6809E microprocessor clocked at rates up to 2 MHz. The interface module adds one ALS TTL load to all monitored lines and an interface capacitance of approximately 35 pF.

Performance Verification and Adjustment Procedures

There are no automatic performance tests or adjustments for the HP 10308B Interface Module.

Troubleshooting

If a failure is suspected in the HP 10308B Preprocessor Interface Module, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

B Analyzing Multiple Microprocessor Systems

The HP 1650A and HP 16510A logic analyzers can be configured to analyze two 6809/6809E microprocessors at the same time. In today's complex systems, this allows you to analyze and debug simultaneous responses from multiple microprocessor systems and correlate data being sent between microprocessors.

To do this you must have two HP 10308B Preprocessors and two HP 10269C General Purpose Probe Interfaces.

1. Install the 6809/6809E Preprocessors (HP 10308B) in the probe interfaces (HP 10269C).

2. Connect the 6809/6809E preprocessor cables to the target systems.

3. Plug the analyzer probes into the probe interfaces as follows:

HP 1650A and 16510A Pod	(into)	HP 10269C Connector
		HP 10269C-1
1		1
2		2
		HP 10269C-2
4		1
5		2

4. Load the logic analyzer configuration and inverse assembler by loading file C6809_I from the inverse assembler disc.

5. Assign Pods 4 and 5 to machine 2 (Analyzer 2) of the logic analyzer.

6. Bring up the Format menu of Analyzer 2 and set up the labels and configuration for pods 4 and 5 as they appear for pods 1 and 2 (see figure B-1).

7. Assign the M clock to pods 4 and 5 the same way the J clock is assigned to pods 1 and 2 (see figure B-1).

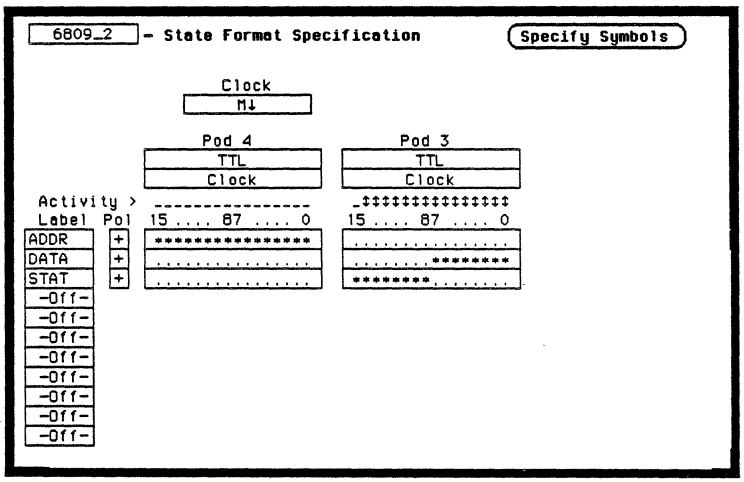

Figure B-1. Format Menu Configured for Two 6809/6809Es

8. Enter the same symbols used in Analyzer 1 for Analyzer 2 (see figure B-2).

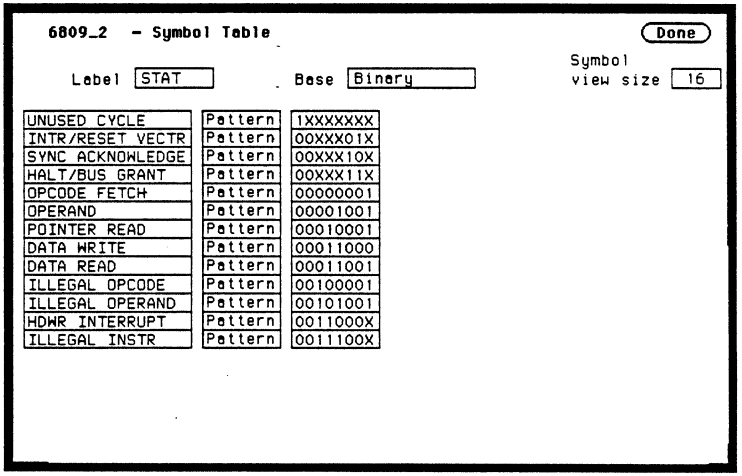

Figure B-2. Symbols Menu for Analyzer 2

9. Press Run to capture the data.

10. Load I6809_I (inverse assembler file) into Analyzer 2 of the logic analyzer.

11. Go to the Display menu for Analyzer 2 and change the base of the data label from hexadecimal (HEX) to "Invasm."

12. This configuration allows you to view each microprocessor's activity individually, or both microprocessors simultaneously, using a "mixed-mode" display. Select the display that is most useful for your application.

13. When you have finished configuring the menu, bring up the Disc menu of the logic analyzer and store this configuration in a separate file for later use.

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